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DEDUCTIVE SWITCH-LEVEL CMOS-VLSI FAULT SIMULATION

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Abstract

The problem of high operational reliability is closely related with testability and self-testing as well as with fault detection test generation and test completeness examination for VLSI and electronics made on such a basis. Generalization of effective bipolar gate structure fault simulation methods is presented, and CMOS fault simulation problems are discussed for an extended class of faults. The class includes stuck-at, transistor stuck-ON and stuck-OFF, breakage, and shortage faults. A through CMOS fault detection method has been proposed for faults to be detected on the input set given. The method differs from concurrent-deductive simulation being familiar in literature, by application of a switch model of a structure analyzed, that does not fit the classic switch simulation theory conceptions.

Key words: fault, simulation, switch level, CMOS, structure, transistor

1 Introduction

Fault simulation is known to be used to examine test quality when designing the test by means of random search method. Bipolar structure fault simulation problem is given much attention in literature. Methods based on deductive simulation ideology [1], [2], are the most effective between well-known ones as applied to gate structures. The deductive simulation method is developed enough to simulate stuck-at faults at the gate representation level [2]-[13] for circuits using Programmable Arrays [14], [15]. However, practically all available simulation methods had become invalid when CMOS technology began to use. It concerns, primarily, to the fault simulation methods based on the gate circuit representation and classic switch simulation theory. To simulate correctly the real CMOS structure faults at logical level, it is required to represent a circuit at so-called switch (transistor) level, because number of effects appeared in these structures can't be specified satisfactory at the gate level of device representation [16], [17]. So in ref. [16] it has been shown that to simulate a break fault F appeared at one input of a NOR element one can specify this case by stuck-at-0 fault model ($\equiv 0$) and detect it on the input set $\{01\}$, what is impossible if the given element is produced using CMOS technology. In this case the abovementioned fault transforms the gate element to a memory element, and to detect the fault one should use fault detection test with length equalled 2. Therefore, the following sequences of sets: {10-00}, {01-00}, or {11-00}, may be used to detect this fault. Hence, the fault simulation at the gate level is physically impracticable. An extensive literature devoted to MOS/CMOS test diagnosis and simulation is presented in ref. [17]. There are gate structure synthesis methods that make it possible to implement device operation modes with presence of certain classes' faults. However, similar methods are not formalized satisfactorily, and practical implementation of them appears to be inexpedient due to both complication of infor-

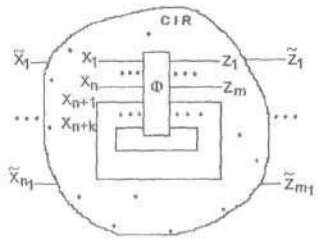

Figure 1: The digital structure CIR: $\tilde{x}_1, ..., \tilde{x}_{n_1}$-structure inputs; $\tilde{z}_1, ..., \tilde{z}_{m_1}$-structure outputs; Φ-one of the function-block structure; $x_1, ..., x_n$-external inputs of the block Φ; $x_{n+1}, ..., x_{n+k}$-block internal-state variables; $z_1, ..., z_m$-block outputs; $A_1, ..., A_{n+k}$-set of faults to be detected at the correspondent inputs of Φ.

mal synthesis and excessive growth of complexity of a structure simulated.

The adequate CMOS-structure simulation problem may be solved satisfactorily at the switch level, where operation of a separate transistor is described by a logical model. Nevertheless, this representation level does not make it possible to solve effectively the fault simulation problem for ICs of modern sizes. Therefore, while solving this problem it is expedient to represent the examined structure at the hierarchical function-switch level with blocks, combined in the framework of the single model, which are represented both at the function-logical level and at the transistor one.

There is a number of papers describing MOS-structure logic simulation at the switch level [16]-[24], nevertheless, fault simulation on this level has received little attention. Something of practical results of parallel fault simulation at the switch level is presented in ref. [24]. Yet known features of gate-structure parallel fault-simulation connected with low efficiency of event simulation process organization are dramatized on the switch simulation level and require of a great quantity of sequential calculations when simulating faulty modifications.

In this paper we represent a generalized concurrent-deductive method of gate-structure fault simulation and propose main formulae for through calculation of extended-class faults for transistor representation of MOS structures. We use a healthy-structure logical model based on representation of the structure simulated by an oriented graph of Petri's network and dynamic increment calculation methods under conditions of dynamical change of the graph structure.

2 Features of Deductive Fault Simulation at the Gate Level

Among gate-level fault-simulation methods known in literature the methods based on the deductive simulation ideology are the most effective ones [1]-[15]. These methods are based on estimation of the given class of faults which are detected in test points of the device immediately at the stage of healthy circuit simulation. In general case the task to calculate the faults specified above reduces to the problem of calculation of fault sets to be detected at the output of some function block of the structure analyzed.

Let us consider the circuit CIR that contains n_1 inputs and m_1 outputs and some test points (Fig.1). Consider generally the estimation method to detect faults by an example of one of the function blocks (the Φ block) of the given circuit. The block is considered to be a finite automaton. Let us denote external inputs of the Φ block possessed by the CIR structure analyzed, by $x_1, x_2, ..., x_n$, the block's outputs by $z_1, z_2, ..., z_m$, and variables, determining the internal state of block with memory (a nontrivial automaton), by $x_{n+1}, x_{n+2}, ..., x_{n+k}$. By the inputs of the sequential-type function block are meant $x_1, x_2, ..., x_n, x_{n+1}, x_{n+2}, ..., x_{n+k}$, whereas the inputs, corresponding to the external input variables, let be $x_1, x_2, ..., x_n$, and vari-

ables of the internal state let be $x_{n+1}, x_{n+2}, ..., x_{n+k}$.

Let us suppose that with applying some input set X_i of the analyzed test $X = X_1, X_2, ..., X_s$ at the inputs of the function block at time t_i, a signal has appeared that is described by the correspondent multivector of length $n+k$. The vector's components correspond to the original variable alphabet, that is accepted to describe a discrete signal in the frame of the model used. Let the original alphabet of variables be $U = \{u_1, u_2, ..., u_g\}$. Assume that fault sets $A_1, A_2, ...A_{n+k}$ to be detected at the correspondent inputs of the block Φ with the given input set X_i of the circuit CIR are associated with the inputs $x_1, x_2, ..., x_{n+k}$. The sets $A_{n+1}, ..., A_{n+k}$ include the faults which had been detected before the moment the input vector under consideration appeared at the external inputs of the block Φ due to fault storage phenomenon. The deductive simulation idea is in following:

1. The output state vector $B_m = (b_1, b_2, ..., b_m)$, $b_1, b_2, ..., b_m \in U$ is determined for a faultless-circuit function block Φ that at the instant t_i of time accepts the input action described by the input vector $\tilde{A}_{n+k} = (a_1, a_2, ..., a_n, a^0_{n+1}, a^0_{n+2}, ..., a^0_{n+k})$. The block Φ was in some initial state $\tilde{A}^0_k = (a^0_{n+1}, a^0_{n+2}, ..., a^0_{n+k})$, $a^0_{n+1}, a^0_{n+2}, ..., a^0_{n+k} \in U$. The external action described by the vector $\tilde{A}_n = (a_1, a_2, ..., a_n)$, $a_1, a_2, ..., a_n \in U$ comes to the external inputs $x_1, x_2, ..., x_n$.

Denote the vector of a new internal state of the block by $\tilde{A}_k = (a_{n+1}, ..., a_{n+k})$, $a_{n+1}, ..., a_{n+k} \in U$. The block response vector is $B_{m+k} = (b_1, ..., b_{m+k})$. It specifies a signals state at the block outputs as well as new values of the block's internal state variables.

2. Using the block transition/output table, the vector subset W_p, $(p = 1, ..., \bar{p})$ is determined from the vector set of output states for the given element type. The states should satisfy the following condition: every vector of the subset W_p should differ from the vector B_m by at least one component having definite value inversed as compared with B_m.

3. The input state vector $\tilde{A}_{n+k}$ is determined for every vector $w_i \in W_p$. At this state the signals specified by w_i are generated.

4. The fault set F to be found on the given test of length s at the block's outputs is calculated as follows:

$$F = \bigcup_{f=\overline{1,S}} \Big(\bigcup_{p=\overline{1,\bar{p}}} \big(\bigcap_{i \in Q_1} A_i \setminus \bigcup_{i \in Q_0} A_j \big) \bigcup e^* \Big), \quad (1)$$

where Q_1 is the set of the block's inputs, which, being in healthy state, accept signals' logic values inversed as compared with correspondent items of the vector $\tilde{A}_{n+k}$; Q_0 the set of inputs, having the same logic values; e^* an internal block fault. Eq. (1) represents an universal model to calculate faults to be detected at the outputs of the function block represented as a digital automaton.

As a rule, practical implementation of the test completeness analysis computation procedures process only binary input vectors at the calculation stage. If no convergent branchings are supposed, the calculation process may be simplified significantly with increasing of the calculation efficiency. Eq. (1) makes it possible to refuse to use the idea of function-block parallel simulation on the number of the input vectors used usually in practice of concurrent-deductive fault simulation, and to replace it by scanning of transition tables presented in proper form.

3 Features of the Switch Simulation Methods

Various transistor-level digital-structure simulation approaches are known in the literature [16], [18]-[24]. In ref. [18]-[20] the CKA-simulation method is proposed, permitting to represent any MOS-structure component by a multiform model and, in a way, to combine these models according to the structure of the circuit to be modelled. The signal is represented by the two-component vector (SS, S), where

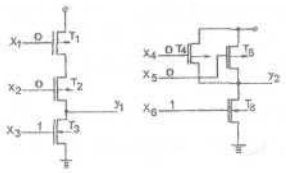

Figure 2: CMOS structure fragments: resistances of the transistors T_1, T_2, T_6 equal 2, those for the transistors T_3, T_4, T_5 are 4.

SS is the signal state ($SS \in \{0, 1, x, z\}$), S is the signal strength ($S = \{1, 2, ...\}$). The significance of the signal representation depends on dimension of the strength value set and determines, to a certain extent, adequacy of the model obtained. The method to determine a static switching-structure node state is proposed in ref. [21]-[24], that is based on search of the path having the least resistance between the node and the source of the fixed signal. However, the path resistance is supposed to be determined by the greatest transistor resistance from amongst the transistors located along the path. So, the resistance of the circuit formed by transistors connected in parallel is determined by the transistor having the least resistance. The resistance of the circuit formed by sequentially connected transistors is determined by the transistor having the largest resistance. This assumption simplifies significantly the calculation procedures, but it can give erroneous results. If transistor resistances of the circuit took the values shown in Fig.2, the signals would be equal 1 at the output y_1 and 0 at the output y_2, but this estimate isn't consistent with what is observed really. The circuitry analysis shows that the two outputs have the intermediate level corresponding to the value of x. This drawback is eliminated in ref. [24] by searching of the shortest path to the node using increment graph algorithms.

In ref. [16] the formal digit structure model has been proposed at the function switch level in term of Petri's modified circuit. Use of such a model makes it possible to reduce the switch circuit simulation to performing the Petri's circuit. The structure-component multiform models suggested in ref. [18]-[20] have been used here. The purpose of this article is to determine the approach to simulate a healthy structure in such a way as to provide the best solution of fault simulation problem and to develop effective method to simulate the faults on this base, rather than to compare the known methods of switch-level digital-structure simulation by function representation adequacy and simulation efficiency. Investigation of this problem has shown that the simulation methods based on global graph algorithm application [21]-[24] are less effective for fault simulation, and, on the contrary, graph increment algorithms (only slightly affecting dynamically the base model) prove to be the most preferable.

4 General Features of the Object Simulated

The elements of the switch circuit are MOSFETs operating as voltage-controlled resistance switches. They connect two nodes with low or high resistance in dependence on their states: "transistor ON" or "transistor OFF". In another way, MOSFET behaves as voltage-controlled nonlinear resistor, in which gate voltage controls resistance between the source and drain nodes. In MOS structure logical functions are made with connectors. Pull-down transistors work as signal commutators, pull-up ones as signal sources. Any transistor is specified by certain resistance to be dependent on the transistor's geometric dimensions and a set of technological parameters and operation conditions. Analog resistance parameters of elements are not taken into account in at explicit form at the switch simulation level as opposite to the circuitry one. Some logical resistance value is assigned to each transistor, to make it possible to correlate and to display in an indirect way conductances of signal paths from the fixed-signal source to the circuit's outputs. The more logical resistance levels are taken into consideration in simulation, the higher is valence of the

simulation algebra and, respectively, precision of the models created.

A MOS structure is considered to be a fixed-signal source commutation system. The structure elements are sources of fixed and alternative signals (power supply sources, grounds, and input signals of the circuit), dynamical-signal sources (capacitive sources), transistors operating in a switch mode, and pull-up transistors. The MOS structure shown in Fig.3 implements XOR function.

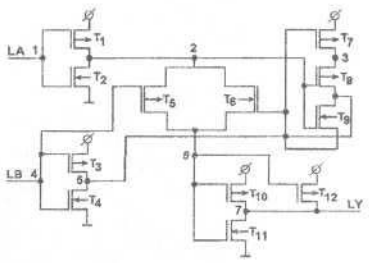

Figure 3: An example of a CMOS structure

5 Digital Structure Fault Simulation at the Switch Level

MOS-structure switch-level functions are formed with connectors that may be modelled by some equipotential surface, where the logical functions are implemented by means of wiring. Let us consider the task to determine the fault set F_i to be detected in some node i of the switch structure STR, when the input vector X_i (Fig.4) is applied. The faults like breakages, "transistor stuck-OFF", "nodes stuck-at", and "transistor stuck-ON" are considered. The connector input lines, $x_1, x_2, ..., x_h$, may be associated at this moment with the fault sets of the given class, $A_1^0, A_1^1, A_1^z, A_1^x, ..., A_h^0, A_h^1, A_h^z, A_h^x$, where the subscripts point at the connector input number, the superscripts indicate the line logical state related with emergence of the fault possessed by the set considered. Thus, for example, A_1^z is the set of STR-structure faults which generate the signal, corresponding to the high impedance, at the given branch of the logical signal state. In a general way the fault set $A_y = \{A_y^1, A_y^0, A_y^z, A_y^x\}$ is associated with the connector's output. The faults occurred in the STR circuit set up the correspondent output-line logical state.

It was mentioned above that in MOS-structures the switch function is made by connectors, which may be modelled by some equipotential surface or wiring logical element. The connector is assumed to be in logical "0" ("1") state, and the input action specified by the vector $E_h = (e_1, e_2, ..., e_h), e_1, e_2, ..., e_h \in U$ comes to the connector's inputs at some instant t (logical-signal strength is supposed to be the same). Suppose $y = e_1 \# e_2 \# e_h = 0$. It is required to determine the fault set F_y^1, setting up the state "1" in this node, i.e. the faults to be detected here. Furthermore, F_y^x and F_y^z are to be detected. It is apparent that to determine F_y^1, F_y^x and F_y^z one may use eq. (1) to describe the connector as a digital automaton. In this case A_i, A_j are supposed to be a set of faults which change a line logic state to a new value possessed by the set $U = \{1, 0, x, z\}$ rather than a fault set to be determined at the correspondent connector input.

Let us consider in more detail calculation of the fault set associated with a switch pull-down transistor output. The switch-type MOSFETs are known to be bidirectional. The direction of

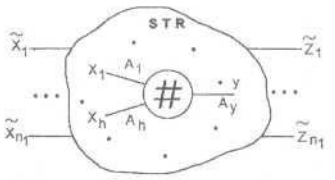

Figure 4: A connector as a logical element of MOS structure.

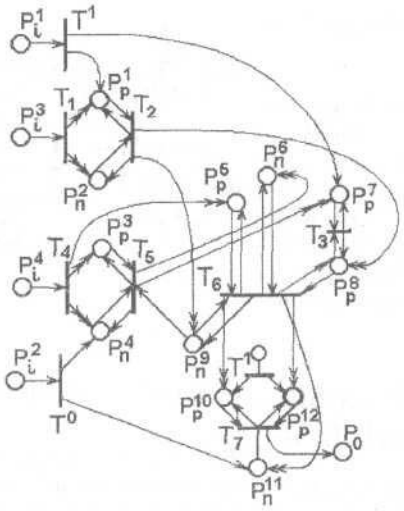

Figure 5: The modified Petri's network

signal propagation is determined dynamically. In a general way, it depends on both the transistor location in the circuit and incoming external signals. For the open transistor the direction of signal propagation is known at every instant of time. The signal is believed to propagate from the node having greater signal strength to another one with less strength level.

Let us denote transistor's outputs as follows: g - gate, s - source, d - drain. Every node connected with the transistor is associated with sets of given class of faults, changing the state of the correspondent line at the instant given. Let the signal $\{g,s\} = \{0,0\}$ or $\{g,s\} = \{0,1\}$ comes to n-type transistor inputs. In this case the transistor will be closed, and to model its output state as z seems to be reasonable. Denote F_d^0 the set of faults which can alter the state of the transistor output d to 0, F_d^1 to 1, and F_d^x to x. F_d^0, F_d^1, and F_d^x are introduced as follows:

- for the combination $\{g,s\} = \{0,0\}$

$$\begin{aligned} F_d^0 &= \Big(F_g^1 \setminus (F_s^1 \cup F_s^z \cup F_s^x)\Big) \cup e^k \\ F_d^x &= \Big(F_g^x \setminus (F_s^1 \cup F_s^z)\Big) \cup (F_g^1 \cap F_s^x) \\ F_d &= \{F_d^0, F_d^x\}; \end{aligned} \tag{2}$$

- for the combination $\{g,s\} = \{0,1\}$

$$\begin{aligned} F_d^0 &= F_g^1 \cap F_s^0 \\ F_d^1 &= e^k \\ F_d^x &= \Big(F_g^x \cap (F_s^0 \cup F_s^x)\Big) \cup (F_g^1 \cap F_s^x) \\ F_d &= \{F_d^0, F_d^1, F_d^x\}, \end{aligned} \tag{3}$$

where F_g^* and F_s^* are fault sets which cause logical "1" to appear a logical state $* \in \{0,1,x,z\}$ at the line g or s; e^k the "transistor stuck-ON" fault.

Assume that the set $\{g,s\} = \{1,0\}$ or $\{g,s\} = \{1,1\}$ comes to the n-type transistor input. For the case $\{g,s\}$ - $\{1,0\}$:

$$\begin{aligned} F_d^z &= F_g^0 \bigcup F_g^z \bigcup F_s^z \bigcup F_s^1 \bigcup e^z \\ F_d^x &= \Big(F_g^x \backslash (F_s^z \bigcup F_s^1)\Big) \bigcup \Big(F_s^x \backslash (F_g^z \bigcup F_g^0)\Big) \\ F_d &= \{F_d^z, F_d^x\}, \end{aligned} \tag{4}$$

where e^z the internal "transistor stuck-OFF" fault.

For the set $\{g,s\}$ - $\{1,1\}$:

$$\begin{aligned} F_d^1 &= e^k \\ F_d^0 &= F_s^0 \backslash (F_g^0 \bigcup F_g^x \bigcup F_g^z) \\ F_d^x &= \Big(F_g^x \bigcap (F_s^0 \bigcup F_s^x)\Big) \bigcup \Big(F_s^x \backslash (F_g^0 \bigcup F_g^z)\Big) \\ F_d &= \{F_d^1, F_d^0, F_d^x\}. \end{aligned} \tag{5}$$

By analogy, one can write the equations to calculate the fault sets F_d^0, F_d^1, F_d^x and F_d^z to be detected at the output d of a p-type pull-down transistor. For the transistor to be used as a load the following equations are valid when the fixed signal $\alpha \in \{1,0\}$ comes to the input X from a fixed signal source:

$$\begin{aligned} F_y^z &= e^z \bigcup F_x^z \\ F_y^\alpha &= e^k. \end{aligned} \tag{6}$$

Eqs. (1)-(6) make it possible to carry out through calculation of the expanded class of the fault sets to be determined in the given test at the stage of simulation of a healthy digital structure represented at the function-switch level. For this purpose the structure of Fig.4 is presented as a modified Petri's network (Fig.5). The structure simulation is reduced to performance of the Petri's network [16]. Calculation of faults to be determined is carried out in accordance with eq. (1) - (6) at the stage of calculation of the network marks.

6 Conclusion

The approach proposed to simulate MOS-structure faults at the expanded fault class makes it possible to carry out analysis of digital circuit test completeness that is comparable with gate-level fault simulation.

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