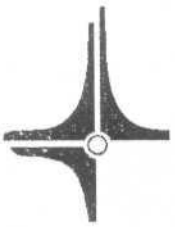

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DYNAMIC - LOGIC SIMULATION ALGORITHM OF SWITCH MOS - STRUCTURES

LUDMILA ZOLOTOREVICH

Belarusian State University, Department of Applied Mathematics and Informatics, Minsk, Belarus, tel. (0172)2265881, e-mail: zolotorevich@fpm.bsu.unibel.by

Abstract. It is being examined here a task of digital MOS-structures simulation at the switch level with signal propagation delays consideration. Simulation is being realized on a basis of a modified time Petri net according to a being simulated circuit structure. Therewith the circuit functioning algorithms are not built in the network structure which limits its complexity by the number of components. The distinguishing feature of the proposed net is the introduced system of the two-level marking of the net elements by means of which a row of being simulated circuit functional parameters is calculated.

Key Words: simulation, MOS-structure, switch level, Petri net, bichromatic oriented multigraph

1. INTRODUCTION

Microelectronics as a branch of industry has that special feature that mathematical simulation is the only instrument to explore projects whether the industrial products functioning is correct on every single designing stage. Therewith because of a very large task dimension the means applying for the simulation must provide the needed compromise between the models precision and the simulation speed on every simulation stage. For exploring a project in the whole on the final designing stage logical simulation methods and dynamic simulation on a switch level are applied. The most actual nowadays from both theoretical and practical points of view is digital MOS-structures dynamic simulation on a switch level. Well known approaches to switch structures simulation published in works [1-11] are based on the presentation of a switch structure as a source signals commutation system with circuit outputs and the correlation of signals propagation circuits resistances. But in the works mentioned the problem of time simulation is not examined and the quasistatistic circuit simulation process is not formalized enough as a whole.

In the present work the task of reducing of MOS-structure time simulation process to constructing and executing of the modified Petri net is set. The initial data are circuit structure, signal propagation delays from sources to circuit nodes.

2. SET-THEORETICAL PRESENTATION OF MODIFIED PETRI NET

Petri net $\Pi = (T, P, I, I^*, O, Q, V, \mu)$, where $T = \{ T^n, T^p, T^d, T^i \}$, $P = (P^1, P^2)$, $T \cap P = \emptyset$. The set T of transitions describes n-type transistors (T^n), p-type transistors (T^p), load transistors (T^d), signal sources (T^i). The set P of positions describes connection lines (the simulation structure nodes); P^1 – input nodes for the examining structure and nodes connected with gates of some transistors; P^2 –all the rest circuit nodes; I, I^* – the input functions of reflection from transitions to sets of positions. I – the function of inputs which describes positions for each transition being input positions for the given transition; I^* - indicates for each transition that input position that corresponds to the operating signal formation node for the given transistor (while describing I function the given position is not indicated); O – the output function of reflection from transitions to the sets of positions, indicates output positions of each transition; Q – the correspondence function of transitions and transistor power parameters. It sets a correspondence to each transition $t_i \in T^{npd}$ ($T^{npd} = T^n \cup T^p \cup T^d$) the logical resistance values of a corresponding transistor. V – the correspondence function of positions input arcs $p_i \in P^1$ and time parameters; μ – two-level network marking.

3. GRAPH-THEORETICAL PRESENTATION OF MODIFIED PETRI NET

Graph-theoretical presentation of the proposed modified Petri net is a bichromatic oriented multigraph where signal sources and structure transistors are described by transitions, and connection lines (structure nodes) – by positions [13-17]. Bounding arcs may have a direction from a transition to a position and from a position to a transition. Each position may be connected by arcs with a row of transitions (fig.1), the number of which is limited by the producing technology of a being simulated device. A transition may be

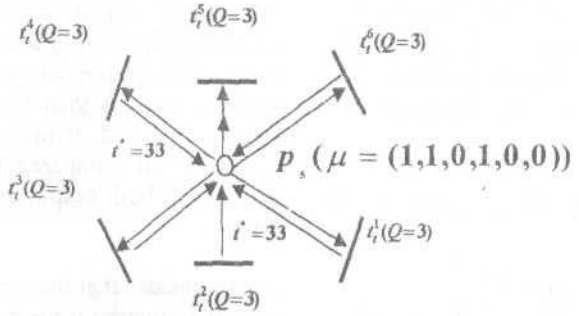

Fig.1. To the illustration of a network marking system

connected with no more than three positions (fig.2, a). At the same time a transition which describes a signal source is connected with only one position (fig.2, b).

A transition may be connected with two positions if it describes a load type transistor (fig.2, c). A position is connected with transitions by an input arc marked with two arrows if it corresponds to a node connected with the gate of a transistor described by a given transition (watch the arc $P_5 - t_t^5$ in fig.1).

With each network position and also with every transition output arc the four-elements vector-marker of logical state $S = (0^{\alpha}, 0.^{\beta}, 1^{\delta}, 1.^{\varepsilon})$ and a time parameter t indicating the moment of logical state S appearance are connected; $\alpha, \beta, \delta, \varepsilon \in (1, \ldots, 100)$, where

0^{α} - a signal logical state on a communication line with the ground source (the signal 0 source is connected with a given node through a chain of transistors being in the open state);

$0.^{\beta}$ - a signal logical state on a possible communication line with the ground source (the signal 0 source is connected with a given node through a chain of transistors being in the open or undefined state);

1^{δ} - a signal logical state on a communication line with the feed source (the signal 1 source is connected with a given node through a chain of transistors being in the open state);

$1.^{\varepsilon}$ - a signal logical state on a possible communication line with the feed source (the signal 1 source is connected with a given node through a chain of transistors being in the open or undefined state).

Above all the statistic time parameter t_c is connected with each input arc of a position from P^1 set.
On fig.3 is quoted an example of a switch structure realizing the equivalence function and on fig.4 – the corresponding to it modified Petri net orgraph.

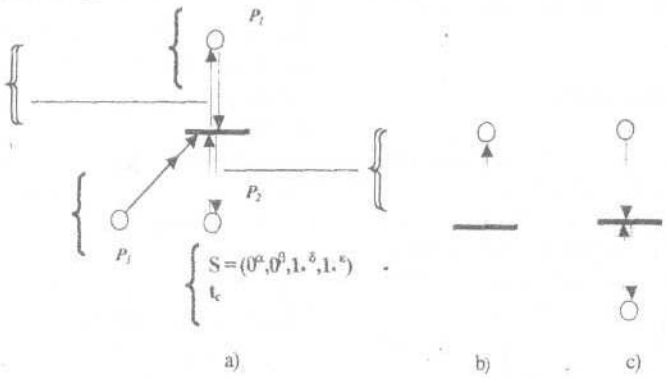

Fig.2. The fragments of the modified Petri net

4. LOGICAL STATE VECTOR-MARKER. ALPHABET OF SIMULATION

The applying simulation alphabet includes symbols from $V \in \{0,1, x, z\}$ set, where 0 and 1 - zero and one logical states, x – vagueness state, z – high impedance logical state. Set V of symbols may be partially regulated: $z < 0 \le 1 < x$. Each signal logical state is additionally described by a signal force from $L = \{1,2, \ldots , n\}$; $n = 100$ (is chosen according to the simulation tolerance). So, the applying alphabet has the following view:

$$A=\{0^{100},1^{100},u^{100},0^{99},1^{99},u^{99},\ldots 0^{i-1},1^{i-1},u^{i-1},\ldots 0^{1},1^{1},u^{1},z\}$$

To speak to the point the alphabet quoted above does not principally differ from the alphabet applied in J.P.Hayes's works [1-5] where the number of symbols is chosen from the simulation tolerance demands. The only distinction is that by Hayes the higher the signal force the lower the force parameter value. Applying in the given work simulation alphabet does not also differ from the alphabet applied in D.Adler's works [10,11]:

$$\psi_{\epsilon} = (s_0, s_1, \ldots, s_n, s_{n+1}, \ldots, s_{2n}, s_{2n+1})$$
$$s_0 < s_1 < \ldots < s_{2n+1}$$

where s_0 means z state (the logical signal power on the line being switched off from the constant signal source); s_{2n+1} - the constant source signal power.

In comparison with Adler's method [10,11] where a signal logical state is identified by the three-element vector $S = (S_{def}, S_0, S_1)$, where S_{def} - the power of the most powerful constant source signal, in the present work with this aim the four-elements vector $S = (0^{\alpha}, 0^{\beta}, 1^{\delta}, 1^{\varepsilon})$ is applied. The using of the given vector allows us to simplify the simulation algorithm.

5. TRANSITIONS START RULES

The start of transitions being started unconditionally (the transitions from T^1 set) is reduced to the illustration of the logical state vector-marker and the time parameter both corresponding to the being started transition output arc. The given vector-marker has the maximum signal force from a constant or an alternative source. For a single S = (0, 0, 100, 100), for a zero - S = (100, 100, 0, 0).

The enabled transition start is realized in the following way:

On 1 stage the states of the input positions current vector-markers being described by 1 input function (P_1 and P_2 on fig.2) are compared. Under 1 condition if all the parameters of one vector-marker (for example, corresponding to P_1) more than the corresponding parameters of another vector-marker (related to P_2) then the output arc for the given transition for which it is necessary to calculate a vector-marker on 2 stage (the arc going from the transition to P_2) is defined. Under condition 2 if comparing vector-markers have all the same parameters then the transition start on the given stage is finished. If the vector-markers of input positions are not compared then on 3 stage the vector-markers of both output arcs will be calculated (3 condition).

Let's consider that the vector-markers of two positions are not compared if the corresponding nodes have connection with different signal sources.
On 2 stage is defined the rule of the calculation of output arcs vector - markers new values planned on 1 stage by the vector-marker parameter value of the input arc connected with the being started transition by the double arrow:

- when $S = (\alpha, \beta, 0, 0)$ $(\alpha \neq 0, \beta \neq 0)$ and when $S = (\alpha, \beta, \delta, \varepsilon)$ $(\alpha \neq 0, \beta \neq 0, \delta \neq 0, \varepsilon \neq 0)$, $\alpha - \delta > a_{min}$, $\alpha - \varepsilon > a_{min}$ (the signal power from the ground source is much higher than the power of possible signals from the feed source), $t \in T^p$; $S = (0,0, \delta, \varepsilon)$ $(\delta \neq 0, \varepsilon \neq 0)$ and when $S = (\alpha, \beta, \delta, \varepsilon)$ $(\alpha \neq 0, \beta \neq 0, \delta \neq 0, \varepsilon \neq 0)$, $\delta - \alpha > a_{min}$, $\delta - \beta > a_{min}$ (the signal power from the feed source is much higher than the power of possible signals from the ground source), $t \in T^n$ - the new values of output arc vector-marker parameters are calculated by means of subtraction of Q parameter, corresponding to the being started transition, from each parameter $a_i \neq 0$ of the vector-marker of the corresponding input position. (Therewith if the new value of the parameter $b_j \le 0$, then $b_j := 0$;
- when $S = (\alpha, \beta, 0, 0)$ $(\alpha \neq 0, \beta \neq 0)$ and when $S = (\alpha, \beta, \delta, \varepsilon)$ $(\alpha \neq 0, \beta \neq 0, \delta \neq 0, \varepsilon \neq 0)$, $\alpha - \delta > a_{min}$, $\alpha - \varepsilon > a_{min}$, $t \in T^n$ $S = (0,0, \delta, \varepsilon)$ $(\delta \neq 0, \varepsilon \neq 0)$ and when $S = (\alpha, \beta, \delta, \varepsilon)$ $(\alpha \neq 0, \beta \neq 0, \delta \neq 0, \varepsilon \neq 0)$, $\delta - \alpha > a_{min}$, $\delta - \beta > a_{min}$, $t \in T^p$ zero parameter values of the output arc vector-marker are set and $S = (0, 0, 0, 0)$;
- when $S = (\alpha, \beta, \delta, \varepsilon)$ $(\alpha \neq 0, \beta \neq 0, \delta \neq 0, \varepsilon \neq 0)$, $|\delta - \alpha| \le a_{min}$ (the powers of signals on the open transistor chains are commensurable by value), or $\delta - \alpha > a_{min}$, $\delta - \beta \le a_{min}$, or $\alpha - \delta > a_{min}$, $\alpha - \varepsilon \le a_{min}$, - new values of the parameters β and ε of the output arc vector-marker are calculated by means of subtraction of Q parameter, connected with the transition being started, from the corresponding by its value vector-marker parameter of the corresponding input position. With $\alpha := 0$, $\delta := 0$. If a new value of parameters $\beta \le 0$, then $\beta := 0$, $\varepsilon \le 0$, then

$\varepsilon := 0$.

On stage 3 output arc vector-marker new values are calculated by the rules which were defined on stage 2. Above all, the time parameter new value is calculated.

On stage 4 is realized the calculation of an output position new vector-marker if the logical state of the arc which is input for the given position was changed. Its noteworthy that the change of vector-marker parameters does not lead without fail to the change of a signal logical state because only a signal source power may be changed and the signal logical state under these conditions may stay the same.

On stage 5 new transitions are allowed to be started if the change of the position vector-marker parameters led to the change of the corresponding signal logical state.

On fig.5 is cited the time diagram of the switch system work, depicted on fig.3, and on fig.4 the calculation dynamics of the positions vector-markers of the network corresponding to the being simulated circuit is shown. Being simulated input forces are indicated on fig.4 in the left upper corner.

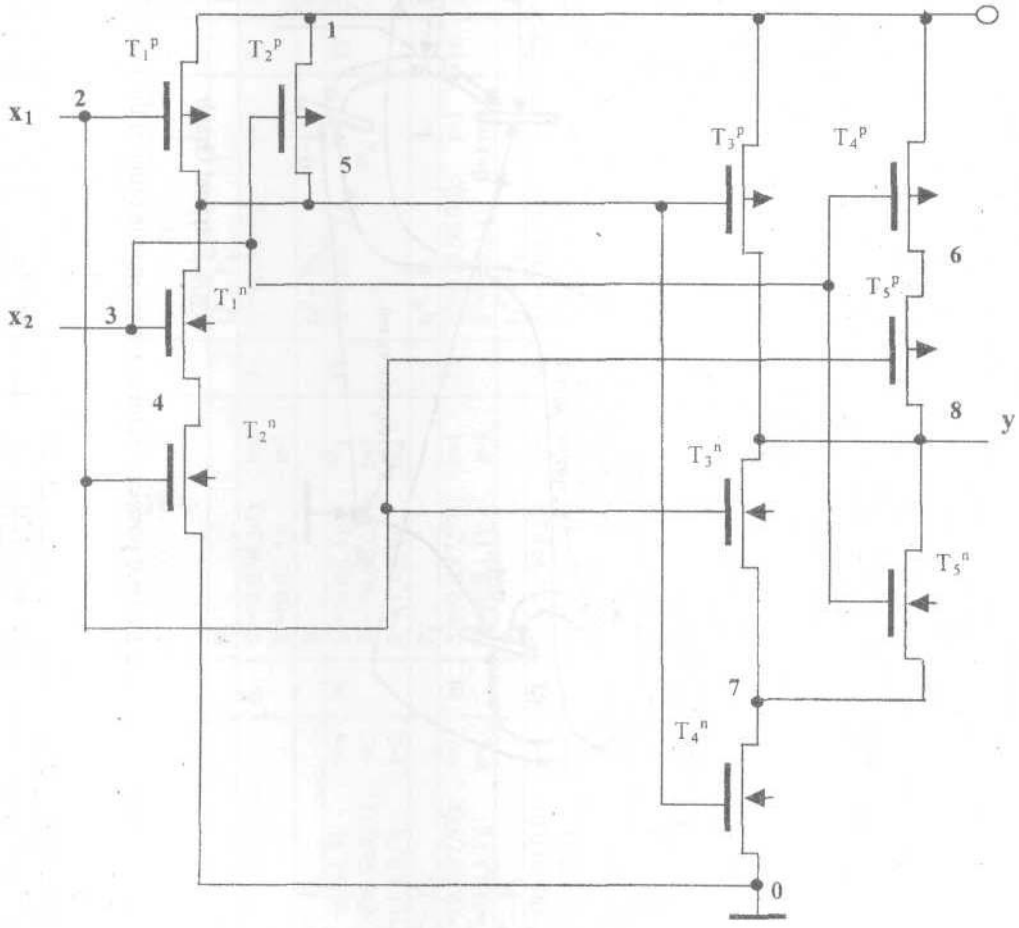

Fig.3. The switch structure realizing the equivalence function

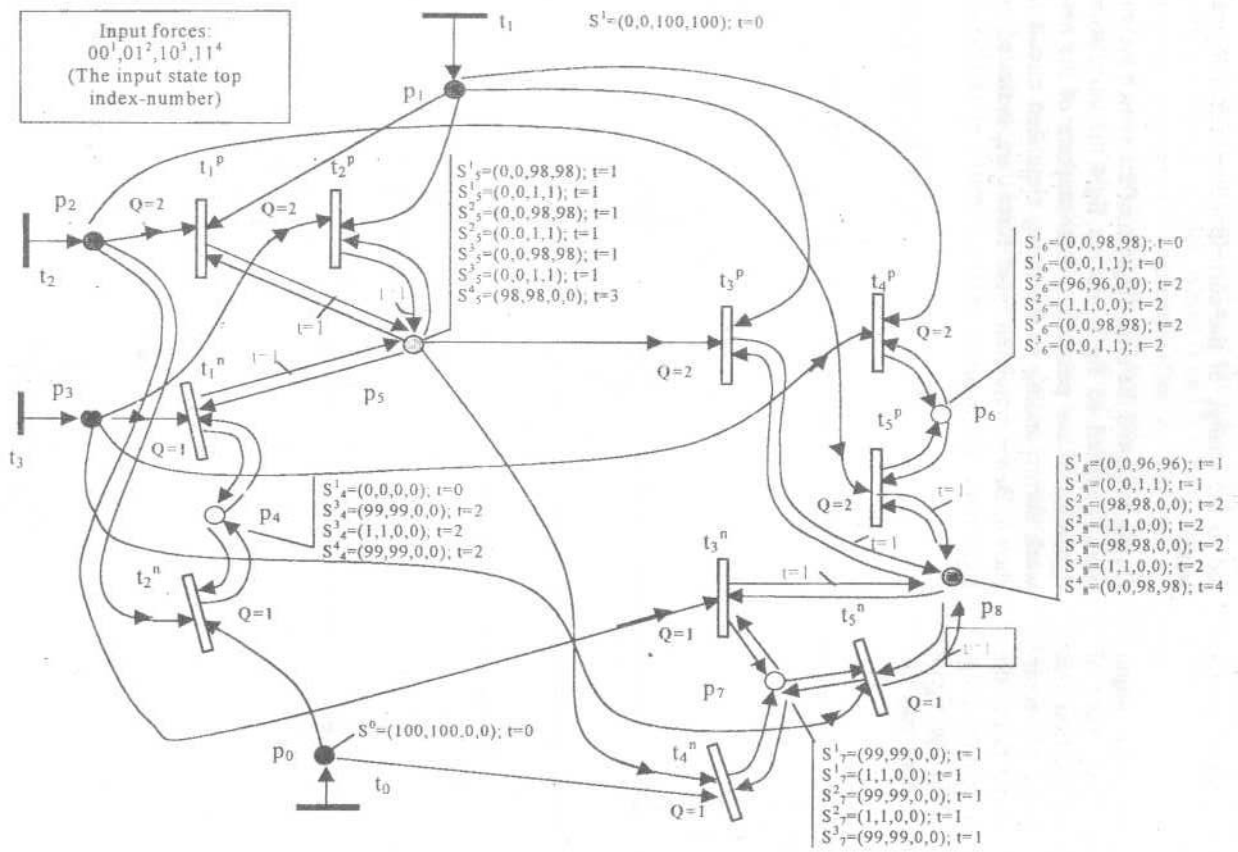

Fig.4. Petri net Graph

Table 1. Output arcs and position vector-markers and the order of their calculation

Input vector – (00)

	$t_0 - P_0$ (P_0)		$t_1 - P_1$ (P_1)		$t_2 - P_2$ (P_2)		$t_3 - P_3$ (P_3)
1	$S^1=(100,100,0,0);\ t=0$	2	$S^1=(0,0,100,100,);\ t=0$	3	$S^1=(100,100,0,0);\ t=0$	4	$S^1=(100,100,0,0);\ t=0$
	$t_1^p - P_5$		P_5		$t_2^p - P_5$		P_5
5	$S^1=(0,0,98,98);\ t=1$ $S^1=(0,0,1,1);\ t=1$	6	$S^1=(0,0,98,98);\ t=1$	7	$S^1=(0,0,98,98);\ t=1$ $S^1=(0,0,1,1);\ t=1$	8	$S^1=(0,0,98,98);\ t=1$ $S^1=(0,0,1,1);\ t=1$

	$t_4^p - P_6$		P_6		$t_5^p - P_8$		P_8	
9	S^1=(0,0,98,98); t=0 S^1=(0,0,1,1); t=0	10	S^1=(0,0,98,98); t=0	11	S^1=(0,0,96,96); t=1 S^1=(0,0,1,1); t=1	12	S^1=(0,0,96,96); t=1 S^1=(0,0,1,1); t=1	
	$t_5^p - P_6$		P_6		$t_4^n - P_7$		P_7	
13	S^1=(0,0,94,94); t=1 S^1=(0,0,1,1); t=1	14	S^1=(0,0,98,98); t=0 S^1=(0,0,1,1); t=0	15	S^1=(99,99,0,0); t=1 S^1=(1,1,0,0); t=1	16	S^1=(99,99,0,0); t=1 S^1=(1,1,0,0); t=1	

Input vector –(01)

	$t_2 - P_2$ (P_2)		$t_3 - P_3$ (P_3)		$t_1^p - P_5$		P_5	
1	S^2=(100,100,0,0); t=1	2	S^2=(0,0,100,100,); t=1	3	S^2=(0,0,98,98); t=1 S^2=(0,0,1,1); t=1	4	S^2=(0,0,98,98); t=1 S^2=(0,0,1,1); t=1	
	$t_2^p - P_5$		P_5		$t_4^p - P_6$		P_6	
5	S^2=(0,0,0,0); t=2	6	S^2=(0,0,98,98); t=1 S^2=(0,0,1,1); t=1	7	S^2=(0,0,0,0); t=1	8	S^2=(0,0,1,1); t=1	
	$t_5^p - P_6$		P_6		$t_5^p - P_8$		P_8	
9	S^2=(0,0,1,1); t=1 S^2=(96,96,0,0); t=2 S^2=(1,1,0,0); t=2	10	S^2=(0,0,1,1); t=1 S^2=(96,96,0,0); t=2 S^2=(1,1,0,0); t=2	11	S^2=(0.0,1,1); t=1	12	S^2=(0,0,1,1); t=1	
	$t_1^n - P_4$		P_4		$t_1^n - P_5$		P_5	
13	S^2=(0,0,97,97); t=1 S^2=(0,0,1,1); t=1	14	S^2=(0,0,97,97); t=1 S^2=(0,0,1,1); t=1	15	S^2=(0.0,96,96); t=1 S^2=(0,0,1,1); t=1	16	S^2=(0,0,98,98); t=1 S^2=(0,0,1,1); t=1	
	$t_4^n - P_7$		P_7		$t_5^n - P_8$		P_8	
17	S^2=(99,99,0,0); t=1 S^2=(1,1,0,0); t=1	18	S^2=(99,99,0,0); t=1 S^2=(1,1,0,0); t=1	19	S^2=(98,98,0,0); t=2 S^2=(1,1,0,0); t=2	20	S^2=(98,98,0,0); t=2 S^2=(1,1,0,0); t=2	

Input vector –(10)

	$t_2 - P_2$ (P_2)		$t_3 - P_3$ (P_3)		$t_1^p - P_5$		P_5	
1	S^3=(0,0,100,100); t=2	2	S^3=(100,100,0,0); t=2	3	S^3=(0,0,0,0); t=2	4	S^3=(0,0,1,1); t=1	
	$t_2^p - P_5$		P_5		$t_1^n - P_5$		P_5	
5	S^3=(0,0,98,98); t=2 S^3=(0,0,1,1); t=2	6	S^3=(0,0,98,98); t=1	7	S^3=(0,0,0,0); t=1	8	S^3=(0,0,98,98); t=1 S^3=(0,0,1,1); t=1	
	$t_1^n - P_4$		P_4		$t_2^n - P_4$		P_4	
9	S^3=(0,0,0,0); t=2	10	S^3=(0,0,0,0); t=1	11	S^3=(99,99,0,0); t=2 S^3=(1,1,0,0); t=2	12	S^3=(99,99,0,0); t=2 S^3=(1,1,0,0); t=2	
	$t_4^p - P_6$		P_6		$t_5^p - P_8$		P_8	
13	S^3=(0,0,98,98); t=2 S^3=(0,0,1,1); t=2	14	S^3=(0,0,98,98); t=2 S^3=(0,0,1,1); t=2	15	S^3=(0,0,0,0); t=2	16	S^3=(0,0,0,0); t=2	
	$t_5^n - P_8$		P_8		$t_3^n - P_7$		P_7	
17	S^3=(1,1,0,0); t=0	18	S^3=(1,1,0,0); t=2	19	S^3=(1,1,0,0); t=2	20	S^3=(1,1,0,0); t=0	
	$t_4^n - P_7$		P_7		$t_3^n - P_8$		P_8	
21	S^3=(99,99,0,0); t=2 S^3=(1,1,0,0); t=2	22	S^3=(99,99,0,0); t=1 S^3=(1,1,0,0); t=1	23	S^3=(98,98,0,0); t=2 S^3=(1,1,0,0); t=2	24	S^3=(98,98,0,0); t=2	
	$t_5^n - P_7$		P_7		$t_5^n - P_8$		P_8	

25	S^3=(0,0,0,0);	t=2	26	S^3=(99,99,0,0); S^3=(1,1,0,0);	t=1 t=1	27	S^3=(0,0,0,0);	t=2	28	S^3=(98,98,0,0); S^3=(1,1,0,0);	t=2 t=2

Input vector –(11)

	$t_2 - P_2$ (P_2)			$t_3 - P_3$ (P_3)			$t_2^p - P_5$			P_5	
1	S^4=(0,0,100,100);	t=2	2	S^4=(0,0,100,100);	t=2	3	S^4=(0,0,0,0);	t=3	4	S^4=(0,0,1,1);	t=1
	$t_4^p - P_6$			P_6			$t_5^p - P_6$			P_6	
5	S^4=(0,0,0,0);	t=3	6	S^4=(0,0,1,1);	t=2	7	S^4=(0,0,0,0);	t=2	8	S^4=(0,0,1,1);	t=2
	$t_1^n - P_5$						$t_2^n - P_4$			P_4	
9	S^4=(1,1,0,0);	t=3	10	S^4=(0,0,1,1);	t=1	11	S^4=(99,99,0,0);	t=2	12	S^4=(99,99,0,0);	t=2
	$t_3^n - P_8$			P_8			$t_4^n - P_7$			P_7	
13	S^4=(1,1,0,0);	t=2	14	S^4=(1,1,0,0);	t=2	15	S^4=(1,1,0,0);	t=1	16	S^4=(1,1,0,0);	t=1
	$t_3^n - P_8$			P_8			$t_1^n - P_5$			P_5	
17	S^4=(1,1,0,0);	t=2	18	S^4=(1,1,0,0);	t=2	19	S^4=(98,98,0,0);	t=3	20	S^4=(98,98,0,0);	t=3
	$t_4^n - P_7$			P_7			$t_3^n - P_8$			P_8	
21	S^4=(0,0,0,0);	t=3	22	S^4=(1,1,0,0);	t=1	23	S^3=(0,0,98,98);	t=4	24	S^3=(0,0,98,98);	t=4

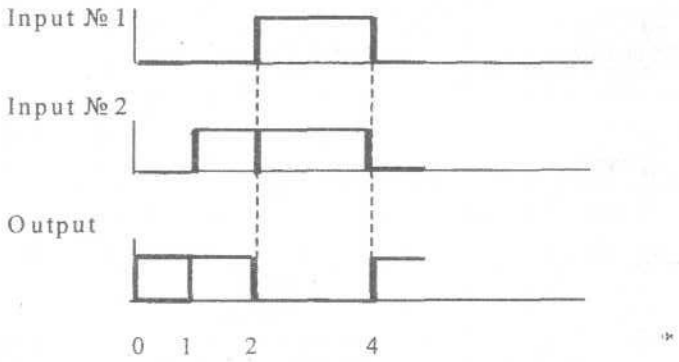

Fig.5. The representation of the results, cited in Table 1, in the form of time diagram

On the time diagram by №2 input (watch fig.5) at the moment 2 there is the change of the signal from 1 into 0 and simultaneously its returning to 1 stage. It occurred as a result of that that the time of feeding of a new input state on the circuit is the moment of transitional process finishing, appeared as a reaction on the previous input state. In this case the input state (10), feeded on the circuit at the moment 2, does not cause any transitional process in the circuit. Therefore at the same moment the next input state (11) is feeded on the circuit.

It's worth mentioning that in the frame of the proposed switch structure simulation method the phenomena of high frequency signal cut-off may be considered. To do that on the stage of the position new value calculation the value of inertial variable should be taken into consideration.

5. CONCLUSION

The cited above algorithm of switch structure simulation on a switch level, based on the corresponding Petri net execution, is mainly intended for the functional verification of projects restored from a topological draught.

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